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What Is Claimed Is:

- 1      Claim 1.    A method for reducing power utilized by a processor comprising the steps of:
  - 2      determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled, and
  - 3      reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.
- 1      Claim 2.    A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprising monitoring a stop clock signal.
- 1      Claim 3.    A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.
- 1      Claim 4.    A method as claimed in Claim 3 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled further comprises providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.
- 1      Claim 5.    A method as claimed in Claim 1 further comprising the steps of transferring operation of a voltage regulator furnishing core voltage in

3 a mode in which power is dissipated during reductions in core voltage to  
4 a mode in which power is saved during a voltage transition when it is  
5 determined that a processor is transitioning from a computing mode to a  
6 mode in which system clock to the processor is disabled.

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1 Claim 6. A method as claimed in Claim 5 further comprising the steps  
2 of returning the voltage regulator to its original mode of operation when  
3 the lower value of the core voltage is reached

1 Claim 7. A circuit for providing a regulated voltage to a processor  
2 comprising:

3 a voltage regulator having:

4 an output terminal providing a selectable voltage, and

5 an input terminal for receiving signals indicating the  
6 selectable voltage level;

7 means for providing signals at the input terminal of the voltage  
8 regulator for selecting a voltage for operating the processor in a  
9 computing mode and a voltage of a level less than that for  
10 operating the processor in a computing mode.

1 Claim 8. A circuit as claimed in Claim 7 in which the means for  
2 providing signals at the input terminal of the voltage regulator comprises  
3 means for accepting binary signals indicating different levels of voltage.

1 Claim 9. A circuit as claimed in Claim 7 in which the means for  
2 providing signals at the input terminal of the voltage regulator comprises:

3 selection circuitry,  
4 means for furnishing a plurality of signals at the input to the  
5 selection circuitry, and  
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means for controlling the selection by the selection circuitry.

1 Claim 10. A circuit as claimed in Claim 9 in which:

2 the selection circuitry is a multiplexor, and  
3 the means for controlling the selection by the selection circuitry  
4 includes a control terminal for receiving signals indicating a  
5 system clock to the processor is being terminated.

1 Claim 11. A circuit as claimed in Claim 7 further comprising means for  
2 reducing the selectable voltage below a level provided by the voltage  
3 regulator.

1 Claim 12. A circuit as claimed in Claim 11 in which the means for  
2 reducing the selectable voltage below a level provided by the voltage  
3 regulator comprises:

4 a voltage divider network joined between the output terminal and a  
5 voltage source furnishing a value higher than the selectable  
6 voltage, and  
7 a voltage regulator feedback circuit receiving a value from the  
8 voltage divider network.

1 Claim 13. A circuit as claimed in Claim 7 further comprising:

2       circuitry for conserving charge stored by the voltage regulator  
3       when the selectable voltage decreases, and

4       means for enabling the circuitry for conserving charge stored by the  
5       voltage regulator when the selectable voltage decreases.

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